REMARKS

By the present amendment, claims 1, 4, 6, and 10 have been amended. Thus, after the present amendment, claims 1-7, 9-11, 13-21, and 32-34 remain in the present application. Reconsideration and allowance of outstanding claims 1-7, 9-11, 13-21, and 32-34 in view of the above amendments and the following remarks are respectfully requested.

A. Rejection of Claims 1-7, 9-11, 13-21, and 32-34 under 35 USC §103(a)

The Examiner has rejected claims 1-7, 9-11, 13-21, and 32-34 under 35 USC §103(a) as being unpatentable over U.S. Patent Number 5,922,065 to Hull, et al. ("Hull") in view of U.S. Patent Number 6,457,173 to Gupta, et al. ("Gupta"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claim 1, is patentably distinguishable over Hull and Gupta, either singly or in combination.

Various embodiments according to the present invention, as defined by amended independent claim 1, relate to decoding very long instruction word (VLIW) packets. Assembly code is provided for each one of a plurality of instructions in a first combination of instructions in a VLIW packet. A template is matched in the VLIW packet to a known template corresponding to one of a plurality of known syntaxes. The plurality of known syntaxes are arranged as a plurality of first level nodes in a tree structure and include programming notation that indicate the end of a particular issue

group. Each of a plurality of second level nodes in the tree structure includes a combination of instruction types. A plurality of paths extends between node levels, and each node of the plurality of first level nodes and the plurality of second level nodes has a path to a node of a different node level. See, for example, Figure 2 of the present application.

Furthermore, each of a plurality of third level nodes in the tree structure includes an instruction type. One of the plurality of known syntaxes is matched with a resolved packet syntax using the tree structure. The resolved packet syntax is used to determine assembly code associated with execution of the first combination of instructions. Assembly code is then provided that is associated with execution of the first combination of instructions.

In addition, programming notations used to refer to the different combinations of execution unit-instruction slot mappings, issue groupings, and chaining of instructions in the exemplary VLIW processor of the present application are a programmer's choice and also depend on the programming language used. For example, when the invention is implemented in the RADL programming language, notations such as "MIIs", "MIsI", "MIsIs", and "MFBs" are used to indicate some of the different combinations of execution unit-instruction slot mappings, issue groupings, and chainings of instructions in the exemplary VLIW processor in the present application.

For example, the programming notation "MIsIs" refers to a VLIW packet having execution unit M assigned to instruction slot 106 and execution unit I assigned to

instruction slot 108. The lower case letter "s" indicates that the first and second instructions located respectively in instruction slots 106 and 108 form a single issue group. According to this exemplary programming notation (i.e. the notation "MIsIs"), execution unit I is assigned to instruction slot 110. Moreover, since there is a "stop" or "s" after the second "I" in programming notation "MIsIs", the instruction located in instruction slot 110 would not be chained to an issue group in the next VLIW packet. In other words, the instruction located in instruction slot 110 is in an issue group by itself.

Accordingly, programming notation "MIsIs" defines a unique known syntax that includes programming notation indicating the end of an issue group, which is then matched with a resolved packet syntax using said tree structure. Thus, claim 1 has been amended to further illustrate aspects of the present invention. In particular, amended independent claim 1 recites "matching a template in said first composite packet to a known template corresponding to one of a plurality of known syntaxes that includes information indicating an end of an issue group." Thus, the invention as defined by amended independent claim 1 allows for the decoding of a first composite packet that contains a plurality of unique chaining and issue grouping information.

In contrast to the present invention as defined by amended independent claim 1, Hull discloses a processor that utilizes a template field for encoding a set of most useful instructions in a wide-word format. The instruction set of the processor comprises instructions that are one of a plurality of different instruction types. The execution units of the processor are also categorized into different types, wherein each instruction may be

executed in one or more of the execution unit types. The instructions are grouped together into 128-bit sized and aligned containers referred to as bundles. Each bundle includes a plurality of instruction slots and a template field that specifies the mapping of the instruction slots to the execution unit types. More importantly, Hull designates a single "S-bit" per bundle of instructions, which "specifies whether an instruction group boundary occurs after the last instruction of the current bundle." See Hull, column 4, lines 11-13.

Nevertheless, as the Examiner acknowledges, Hull does not teach matching a template in a first composite packet to a known template corresponding to one of a plurality of known syntaxes, wherein the plurality of known syntaxes are arranged as a plurality of first level nodes in a tree structure, wherein each of a plurality of second level nodes in the tree structure includes a combination of instruction types, and wherein each of a plurality of third level nodes in the tree structure includes an instruction type. Hull also does not teach that the resolved packet syntax is determined using the known syntax.

Gupta, on the other hand, is directed to the automatic design of VLIW instruction formats. In Gupta, with the use of a computer the design of efficient binary instruction encodings of VLIW instruction formats is automated. The method involves automatically finding compact instruction formats that can express and exploit the full parallelism specified in the underlying processor microarchitecture.

Figure 2 of Gupta illustrates the structure of an if-tree. This if-tree, however, has critical deficiencies. For example, Gupta designates a single bit to the "consume to end-

of-packet" (CEP) bit field. Consequently, Gupta cannot decode particular programming notation, such as "MIsIs" as discussed above, containing more than one CEP (stop) bit. Moreover, this limitation is also found in Hull and is not cured with the use of the if-tree in Gupta since both of these disclosures allocate a single CEP (stop) bit per VLIW packet. In addition, even if Gupta or Hull allowed the use of more than one CEP (stop) bit per VLIW packet, neither disclosure teaches how to decode such VLIW packets.

Therefore, Gupta does not disclose, teach, or suggest the invention as defined by amended independent claim 1, including the step of matching a known template to a plurality of known syntaxes that includes a programming notation indicating the end of an issue group. Furthermore, there is no teaching or suggestion to combine or modify Gupta. Therefore, Gupta, either singly or in combination with Hull, does not disclose, teach, or suggest the present invention as defined by amended independent claim 1.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claim 1, is not taught, disclosed, or suggested by the art of record. Thus, amended independent claim 1 is patentably distinguishable over the art of record. As such, the claims depending from amended independent claim 1 are, *a fortiori*, also patentable for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Conclusion

Based on the foregoing reasons, the present invention, as defined by amended independent claim 1, and the claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, outstanding claims 1-7, 9-11, 13-21, and 32-34 are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance Notice of Allowance directed to all claims 1-7, 9-11, 13-21, and 32-34 remaining in the present application is respectfully requested.

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Respectfully Submitted,
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